## REMARKS/ARGUMENTS

Claims 1-2, 6-10 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Fig. 1 Prior Art, in view of Nakano, 6,147,923, and Hiratsuka et al., 6,453,707. Applicant has not further amended the claims herein and respectfully submits that such rejection is improper for the following reasons.

Nakano et al. discloses in Fig. 1 a voltage boosting circuit for providing the boosted voltage to the word line of a memory device including: a pumping up circuit comprising an NMOS capacitor 13 and a PMOS capacitor 18 connected in series between to boosted voltage VOUT and the output of inverter 32. However, according to the description of the preferred embodiment in Nakano et at., Pumping-up of the voltage VOUT with using the capacitors 13 and 18 is performed by a middle point voltage control circuit 20 and an end point voltage control circuit 30 (column 3, line 49-52), the pumping up circuit should include a middle point voltage control circuit 20 and an end point voltage control circuit 30 to boost the voltage. There is no one embodiment in Nakano et al. to disclose a pumping up circuit without including a middle point voltage control circuit and an end point voltage control circuit. Therefore, the pumping up circuit in Fig. 1 of Nakano et al. for the MOS capacitor 12 in Applicant's Fig. 1 prior art for the purpose of providing faster boosting doesn't teach every element in the present invention, it includes two extra components: a middle point voltage control circuit and an end point voltage control circuit. If proposed modification would render the prior art invention being modified **unsatisfactory for its intended purpose**, then there is no suggestion or motivation to make the proposed modification.

In addition, the Nakano et al. discloses a voltage boosting circuit for use in a semiconductor device such as a memory device. But, in the present invention, the applicant do not adopt to add at least one MOS capacitor 12 (Fig. 1). The applicant replaced the MOS capacitor 12 with a DRAM cell capacitor 21 in Fig. 2. The purpose of the present invention is to use the current DRAM cell as the

charging capacitor of the memory's pumping circuit. However, Nakano et al. fails to disclose the feature of the present application which uses a DRAM cell capacitor 21 to replace the MOS capacitor 22. Hence, the present invention could reduce the capacitor's area of the VPP pumping circuit and save the extra process cost.

Moreover, both of Nakano et al. and Hiratsuka et al., are not able to disclose such feature, which is included a DRAM cell capacitor replace the MOS transistor at least. As the result, neither Nakano et al. nor Hiratsuka et al redeem the deficiency which is the distinction between the present invention and the admitted prior art. Therefore, the citations do not teach or suggest all the claim limitations.

**Conclusion**

In the light of the above remarks, Applicant respectfully submits those pending Claims 1-2, 6-10 and 12-13 as currently presented are in condition for allowance. Applicant has thoroughly reviewed that art cited but relied upon by the Examiner. Applicant has concluded that this cited reference does not affect the patentability of these claims as currently presented. Accordingly, reconsideration is respectfully requested.

Respectfully submitted,

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